REMARKS

In sections 1-3 of the Office Action, the Examiner rejects claim 7 under 35 USC 112, second paragraph, suggesting that there is insufficient antecedent basis for the limitation "the other portion". Claim 7 has been amended accordingly (see above) and now recites "a first portion" and "a second portion". The Applicants believe that this rejection has been overcome.

In sections 4-5, the Examiner rejects claims 7-8 under 35 USC 102(b) as being anticipated by Nakamura et al. (US Patent No. 5,138,145). Moreover, in section 7, claims 1-6 are rejected under 35 USC 103(a) as being unpatentable over the Admitted Prior Art in view of Kishida et al. (US Patent No. 6,361,867) and Choo et al. (US Patent No. 6,297,869). In section 8, claims 7-11 are rejected under 35 USC 103(a) as being unpatentable over Admitted Prior Art in view of Kishida et al. These rejections are respectfully traversed.

Nakamura et al., the Admitted Prior Art, Choo et al., and Kishida et al., standing alone or in combination, fails to disclose, teach, or suggest, *inter alia*, the following features of the claimed invention:

Claim 1: "placing a protecting circuit, connecting with an external circuit, on the glass substrate"; "providing a melting device with a first laser device and a second laser device;" and "melting a predetermined portion of the protecting circuit by the first laser device, and melting a predetermined portion of the glass substrate by the second laser device".

Claim 7: "bonding the first portion of the integrated circuit device to the glass substrate so that a gap is formed between the second portion of the integrated circuit device and an edge of the glass substrate"; and "introducing resin into the gap so that the resin covers the edge of the glass substrate and the integrated circuit device cannot be damaged by the edge of the glass substrate due to the resin".

Nakamura et al discloses a method for producing image sensors with current flow into chip and with simplified chip mounting. The object of Nakamura et al. is to provide an image sensor that can be fabricated without involving complicated wiring work and can be readily adapted to needs for reduced electrode pitch. In Nakamura et al, the resin 16 is applied on the substrate 18, and then the chip 12 is placed on the resin 16.

Nakamura et al does not teach that resin is introduced into the gap formed between the second portion of the integrated circuit device and the edge of the glass substrate, as recited by claim 7 of the present application. For at least this reason, Claim 7 patently defines over the cited art.

Moreover, Nakamura et al. nowhere mentions "melting a predetermined portion of the protecting circuit by the first laser device, and melting a predetermined portion of the glass substrate by the second laser device", as recited by claim 1 of the present application.

Kishida et al discloses a laminated glass substrate structure and its manufacture. In Kishida et al, the method is used for forming a laminated glass substrate. That is, the laser in Kishida is only used to grind the edge

of the glass substrate. Thus, this citation does not disclose that two laser devices are used to melt different portions of the glass substrate.

Choo et al discloses a substrate and a liquid crystal display panel capable of being cut by using a laser and a method for manufacturing the same. In Choo et al, one laser is used to cut the substrate, and another laser is used to grind the edge of the substrate. Thus, this citation does not disclose that two laser devices are used to melt different portions of the glass substrate.

None of AAPA, Kishida et al, Choo et al teach or suggest that the protecting circuit is melted by the first laser device and the glass substrate is melted by the second laser device. That is, even when Kishida et al and Choo et al are combined with AAPA, the prior art does not teach that the protecting circuit is melted by the first laser device and the glass substrate is melted by the second laser device, as recited by claim 1 of the present application.

MPEP 2131 states that a "claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," quoting Verdegaal Bros v. Union Oil Co. of California, 814 F.2d 628, 631 (Fed. Cir. 1987). Under MPEP 2143, to establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Since the cited references do not teach the above-quoted limitations of claim 1 and claim 7, the Applicants believe that claim 1 and claim 7 are patentable. Claims 4-6 are also patentable, at least by virtue of their

dependency from claim 1. Claims 8 and 10-11 are patentable, at least by virtue of their dependency from claim 7.

The Applicants believe that all claims are in condition for allowance and reconsideration of the present application is respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account No. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

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8/4/03
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